REMARKS

Applicant has carefully reviewed the Office Action of January 24, 2005, and offers the following remarks to accompany the above amendments.

Applicant amends claim 9 to establish appropriate antecedent basis for the new task optimized processor. No new matter is added. Claims 1, 2, 3, 8 and 9 are amended to tidy antecedent basis for the claims. Again, no new matter is added.

Claims 1 and 4-14 were rejected under 35 U.S.C. § 102(e) as being anticipated by Hsu. Applicant respectfully traverses. For the Patent Office to establish anticipation, the Patent Office must show where in the reference each and every element of the claim is taught in the reference. Further, the elements of the reference must be arranged as claimed. MPEP § 2131. The requirement for identity between the reference and the claim is a strict requirement with which the Patent Office has not complied in the present application. In particular, Hsu does not teach optimization as recited in the independent claims, nor does Hsu teach moving processing between processors as recited in the independent claims.

Claim 1 recites "undertaking a given channel processing task for a given channel with one processor of a plurality of processors, said one processor optimized for said given channel processing task. . . ." The Patent Office opines that this element is taught at Hsu, col. 6, lines 43-46, col. 7, lines 8-20, and col. 10, lines 37-53. Applicant respectfully traverses. Applicant describes what is meant by "optimized" on page 6, lines 23-27 and page 9, lines 21-24 of the specification. While Applicant is cognizant that limitations in the specification are not read into the claims, the claim language is interpreted in light of the specification, and the specification affects what someone skilled in the art would consider a reasonable interpretation of the claim language. Since the Patent Office is required to give claim elements their broadest **reasonable** interpretation from the point of view of someone skilled in the art (MPEP § 2111), Applicant's explanation of optimized are relevant to the interpretation assigned thereto.

Applicant has studied the cited passages of Hsu and finds no teaching that one processor is optimized for said given channel processing task as recited in claim 1. An electronic word search of Hsu indicates that the words "optimize" and "optimization" are never used in Hsu. Applicant's reading of Hsu likewise reveals nothing that be construed to be the same as optimization. The cited passages do indicate that channels are assigned to processors if the processors have "sufficient" processing power to meet the processing requirements of a service

type. No one skilled in the art would consider the sufficiency of the processing power in Hsu to be equivalent to the optimization recited in the claim. If the Patent Office opines that some other element within Hsu could be construed to be optimization, Applicant requests that such be identified with greater particularity. In the absence of such an identification, Hsu does not teach a claim element. Since Hsu does not teach a claim element, Hsu does not anticipate claim 1. Since the Patent Office has not set forth a proper rejection of claim 1, claim 1 is allowable.

Claim 1 also recites "moving processing of said given channel to a different one of said plurality of processors . . . ." Hsu does not teach this claim element. The Patent Office opines that this element is taught at Hsu col. 9, lines 24-40, col. 10, lines 3-10, and col. 10, lines 48-53. Applicant respectfully traverses this assertion.

Hsu col. 9, lines 24-40 states in full:

> Each of the processors 130, 132, 134, 136 provides processing of data using appropriate software modules of the DSP operational codes stored in the local memory units 138, 140, 142, 144. To manage the operations of each processor, the set of DSP operational codes stored in each local memory space 138, 140, 142, 144 implements a local resource control (LRC) table for managing processing operations of the corresponding processor.
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> The LRC table of each local memory space 138, 140, 142, 144 includes fields for storing data representative of information describing current processing operations of the corresponding processor. The LRC table provides mapping among software modules of the DSP operational codes and the functions required for processing tasks related to different types of services. Each processor releases its resources upon completion of processing of tasks required by a service call and waits for the next service call request to be received.

Thus, while the passage indicates that there is an LRC table that identifies which processor is managing which operations, and there is an indication that the processor releases its resources upon completion of processing tasks, there is no teaching that the process moves from a first processor to a second processor as recited in the claim.

Hsu, col. 10, lines 3-10 states in full:

> Channel assignment status field 182 is used to store channel assignment information used by resource controller 114 to coordinate the data flow paths between the channels, assigned sections of memory pool 156 (FIG. 2), and assigned processors of processing bank 112. The channel assignment information indicates the service calls are assigned to each processor or processors of the processing bank.

Again, this passage deals with channel assignment to a processor or processors. However, once the assignment is made, there is no indication that the channel is moved to another processor as recited in the claim.

Hsu, col. 10, lines 48-53 states in full:

> When the processing power of one processor is sufficient to meet the processing requirements of a service type, pipeline processing is not required and the resource controller 114 selects a single processor from processing bank 112 (FIG. 1) to be the assigned processor for that service type. When the processing power of one processor is not sufficient to meet the processing requirements of a service, resource controller 114 (FIG. 1) selects two or more of the processors 130, 132, 134, 136 or even one and half of the processors to be the assigned processor for that service type and the assigned processors operate in a pipeline mode.
>
> In operation, referring back to FIG. 2, resource controller 114 activates appropriate modules of the DSP operational codes based on service call requirements by pointing to the proper position on the LRC table of selected processors(s). The controller then revises appropriate records of MRC table 115.

Again, this passage deals with channel assignment and how this information is stored. There is no teaching or suggestion in this passage that the processing is moved from one processor to a different processor. While the passage does indicate that two or more processors may be used for a single channel to meet processing power requirements, this is not, under any reasonable interpretation of "moving", the same as the recited moving of claim 1. In short, Hsu does not teach the claim element. Since Hsu does not teach the claim element, claim 1 is not anticipated for this reason as well.

Since claim 1 is not anticipated, claim 1 is allowable. Claims 4-8 depend from claim 1, and are allowable at least for the same reasons.

Claim 9 recites that certain events take place "when said channel processing task changes to a new channel processing task". The Patent Office has not addressed this element in the claim. However, each element of the claim must be shown in the reference to establish anticipation. Since the Patent Office has made no effort to show where this element of the claim is located in Hsu, Hsu cannot anticipate claim 9.

Claim 9 further recites a task optimized processor. The Patent Office opines that this element is taught at Hsu, col. 6, line 65-col. 7, line 2 and col. 10, lines 3-10. Applicant respectfully traverses this assertion. The cited passages do not indicate that the processor is

optimized as that term is used herein. As explained above, "optimized" is not the same as "sufficient". To this extent, Hsu does not show the claim element.

Claim 9 also recites prompting the new task optimized processor to assume processing in response to the channel processing task changing to a new channel processing task. The Patent Office opines that this element is shown at Hsu, col. 6, line 65-col. 7, line 2 and col. 10, lines 3-10. However, the channel assignments discussed in the cited passages are not in response to a channel processing task changing, but are new channel assignments. Thus, Hsu does not teach the recited prompting.

Since Hsu does not teach these three claim elements, Hsu does not anticipate claim 9, and claim 9 is allowable.

Claim 10 recites "a plurality of processors, each optimized for at least one channel processing task. . . ." The Patent Office opines that this element is taught at Hsu, col. 6, lines 43-46, col. 7, lines 8-20, and col. 10, lines 37-53. Applicant respectfully traverses for the reasons discussed above. The cited passages do not teach "optimized" processors as that term is used herein. Thus, claim 10 is not anticipated.

Claims 11-14 depend from claim 10, and are not anticipated at least for the same reasons.

Claim 2 was rejected under 35 U.S.C § 103 as being unpatentable over Hsu in view of Weiss et al. (hereinafter "Weiss"). Applicant respectfully traverses. For the Patent Office to combine references in an obviousness determination, the Patent Office must do two things. First, the Patent Office must articulate a motivation to combine the two references. Second, the Patent Office must support the articulated motivation with actual evidence. *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999). While the range of sources available to support the motivation is large, the range does not diminish the requirement for actual evidence. *Id.* Even if the Patent Office has properly combined the references, to establish *prima facie* obviousness, the combination must still teach or suggest all the claim elements. MPEP § 2143.03.

Applicant initially traverses this rejection because the Patent Office has not supported the motivation to combine the references with the requisite actual evidence. Specifically, the Patent Office asserts that it would be obvious to combine Hsu and Weiss to increase "the efficiency of the system by utilizing a processor that is best suited to process a particular signal." This asserted motivation lacks the evidence required by the Federal Circuit. As such, this motivation is improper. Since the motivation is improper, the combination is improper. Since the

combination is improper, the rejection is improper. Since the Patent Office has failed to set forth a proper rejection, claim 2 is allowable.

Even if the combination is proper, a point which Applicant does not concede, the combination still fails to show a claim element. Specifically, as discussed above, Hsu does not teach several elements of claim 1 from which claim 2 depends. Weiss does not cure these deficiencies. Since the references individually do not teach or suggest the claim elements, the combination of the two references does not teach or suggest the claim elements identified above. Since the combination does not teach or suggest the claim elements, the Patent Office has not established obviousness. Since the Patent Office has not established obviousness, claim 2 is allowable for this reason as well.

Claim 3 was rejected under 35 U.S.C. § 103 as being unpatentable over Hsu in view of Lin et al. (hereinafter "Lin"). Applicant respectfully traverses. The standard for obviousness is set forth above.

Applicant initially traverses the rejection of claim 3 because the Patent Office has not set forth the evidence to support the motivation to combine the references. Specifically, the Patent Office opines that the motivation is to improve "the quality of signal processing." This motivation lacks any evidence in support thereof. As such, this motivation is improper. Since the motivation is improper, the combination is improper. Since the combination is improper, the rejection is improper. Since the Patent Office has failed to set forth a proper rejection, claim 3 is allowable.

Even if the combination is proper, a point which Applicant does not concede, the combination still fails to show a claim element. Specifically, as discussed above, Hsu does not teach several elements of claim 1 from which claim 3 depends. Lin does not cure these deficiencies. Since the references individually do not teach or suggest the claim elements, the combination of the two references does not teach or suggest the claim elements identified above. Since the combination does not teach or suggest the claim elements, the Patent Office has not established obviousness. Since the Patent Office has not established obviousness, claim 3 is allowable for this reason as well.

Applicant requests reconsideration of the rejections in light of the amendments and remarks presented herein. Applicant earnestly solicits claim allowance at the Examiner's earliest convenience.

Respectfully submitted,

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